Ordering number : ENA1210A

SANYO Semiconductors
DATA SHEET

An ON Semiconductor Company

LC87F2932A — CMOS IC FROM 32K byte, RAM 2048 byte on-chip 8-bit 1-chip Microcontroller

Overview

The SANYO LC87F2932A is an 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrates on a single chip a number of hardware features such as 32K-byte flash ROM (onboard programmable), 2048-byte RAM, an on-chip debugger, sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), four 8-bit timers with a prescaler, a base timer serving as a time-of-day clock, day and time counter, a high-speed clock counter, a synchronous SIO interface (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO interface, a UART interface (full duplex), an 8-bit 13-channel AD converter, two 12-bit PWM channels, a system clock frequency divider, frequency variable RC oscillation circuit, and a 26-source 10-vector interrupt feature.

Features

■Flash ROM
- Capable of on-board-programming with wide range, 3.0 to 5.5V, of voltage source.
- Block-erasable in 128-byte units
- Writable in 2-byte units
- 32768 × 8 bits

■RAM
- 2048 × 9 bits

■Minimum Bus Cycle
- 83.3ns (12MHz) V_{DD}=3.0 to 5.5V
- 125ns (8MHz) V_{DD}=2.5 to 5.5V
- 250ns (4MHz) V_{DD}=2.2 to 5.5V

Note: The bus cycle time here refers to the ROM read speed.

* This product is licensed from Silicon Storage Technology, Inc. (USA), and manufactured and sold by SANYO Semiconductor Co., Ltd.

■Minimum Instruction Cycle Time
- 250ns (12MHz) V_{DD}=3.0 to 5.5V
- 375ns (8MHz) V_{DD}=2.5 to 5.5V
- 750ns (4MHz) V_{DD}=2.2 to 5.5V

■Ports
- Normal withstand voltage I/O ports
  Ports whose I/O direction can be designated in 1-bit units 59 (P0n, P1n, P2n, P30 to P33, P70 to P73, P80 to P86, PBn, PCn, PWM2, PWM3, CF2, XT2)
  (Ports P30 to P33 are available in FLGA68K(6.0×6.0) package only.)
- Normal withstand voltage input port 2 (CF1, XT1)
- Reset pins 1 (RES)
- Power pins 6 (V_{SS}1 to 3, V_{DD}1 to 3)

■Timers
- Timer 0: 16-bit timer/counter with two capture registers.
  Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture register) × 2 channels
  Mode 1: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
  Mode 2: 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture register)
  Mode 3: 16-bit counter (with two 16-bit capture register)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
  Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8 bits)
  Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8 bits can be used as PWM.)
- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)
- Base timer
  1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler output.
  2) Interrupts are programmable in 5 different time schemes

■Day and Time Counter
1) With a base timer, it can be used as 65535days + 23hours + 59minutes + 59seconds counter.
2) Interrupts are programmable in 4 different time schemes (day, hour, minute or second).

■High-speed Clock Counter
1) Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz)
2) Can generate output real-time

■SIO
- SIO0: 8-bit synchronous serial interface
  1) LSB first/MSB first mode selectable
  2) Built-in 8-bit baudrate generator (maximum transfer clock cycle=4/3 tCYC)
  3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1-bit units, suspension and resumption of data transmission possible in 1-byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
  Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  Mode 1: Asynchronous serial I/O (half-duplex, 8-data bits, 1-stop bit, 8 to 2048 tCYC baudrates)
  Mode 2: Bus mode 1 (start bit, 8-data bits, 2 to 512 tCYC transfer clocks)
  Mode 3: Bus mode 2 (start detect, 8-data bits, stop detect)

■UART
- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2-bit in continuous data transmission)
- Built-in baudrate generator

■AD Converter: 8 bits × 13 channels

■PWM: Multifrequency 12-bit PWM × 2 channels

■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)
- Noise rejection function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)

■Watchdog Timer
- External RC watchdog timer
- Interrupt and reset signals selectable

■Clock Output Function
1) Outputs clock with a frequency 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 of the source clock of the system clock
2) Outputs clock of the subclock

■Interrupts
- 26 sources, 10 vector addresses

1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/ BT0/BT1/DHMSC
5	00023H	H or L	T0H/INT6
6	0002BH	H or L	T1L/T1H/INT7
7	00033H	H or L	SIO0/UART1 receive
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/T4/T5/PWM2, PWM3

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.

- IFLG (List of interrupt source flag function)

1) Shows a list of interrupt source flags that caused a branching to a particular vector address (shown in the table above).

■Subroutine Stack Levels: 1024 levels (the stack is allocated in RAM)

■High-speed Multiplication/Division Instructions
- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits

- RC oscillation circuit (internal): For system clock
- CF oscillation circuit: For system clock, with internal Rf
- Crystal oscillation circuit: For low-speed system clock, with internal Rf
- Frequency variable RC oscillation circuit (internal): For system clock
  1) Adjustable in ±4% (typ) step from a selected center frequency.
  2) Measures oscillation clock using a input signal from XT1 as a reference.

■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2µs, 2.4µs, 4.8µs, 9.6µs, 19.2µs, 38.4µs, and 76.8µs (at a main clock rate of 10MHz).

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) There are three ways of resetting the HALT mode.
     (1) Setting the reset pin to the low level
     (2) System resetting by watchdog timer
     (3) Occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, RC, X’tal, and frequency variable RC oscillators automatically stop operation.
  2) There are four ways of resetting the HOLD mode.
     (1) Setting the reset pin to the low level.
     (2) System resetting by watchdog timer
     (3) Having an interrupt source established at either INT0, INT1, INT2, INT4, INT5, INT6, or INT7
         * INT0 and INT1 HOLD mode reset is available only when level detection is set.
     (4) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  1) The CF, RC, and frequency variable RC oscillators automatically stop operation.
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are six ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level
     (2) System resetting by watchdog timer
     (3) Having an interrupt source established at either INT0, INT1, INT2, INT4, INT5, INT6, or INT7
         * INT0 and INT1 HOLD mode reset is available only when level detection is set.
     (4) Having an interrupt source established at port 0
     (5) Having an interrupt source established in the base timer circuit
     (6) Having an interrupt source established in the day and time counter circuit

■On-chip Debugger

- Supports software debugging with the IC mounted on the target board (LC87D2932A).
  LC87F2932A has an On-chip debugger but its function is limited.

■Package Form

- QIP64E (14 × 14): Lead-free type
- TQFP64J (7 × 7): Lead-free type
- FLGA68K (6.0 × 6.0): Lead-free type
- FLGA64 (5.0 × 5.0): Lead-free type

■Development Tools

- On-chip debugger: TCB87- TypeB + LC87D2932A

■Programming Boards

Package	Programming boards
QIP64E (14×14)	W87F50256Q
TQFP64J (7×7)	W87F58256TQ7
FLGA68K (6.0×6.0)	W87F58256FL6 * This board is Built To Order. It may take about a month to deliver.
FLGA64 (5.0×5.0)	W87F59256FL5 * This board is Built To Order. It may take about a month to deliver.

■Flash ROM Programmer

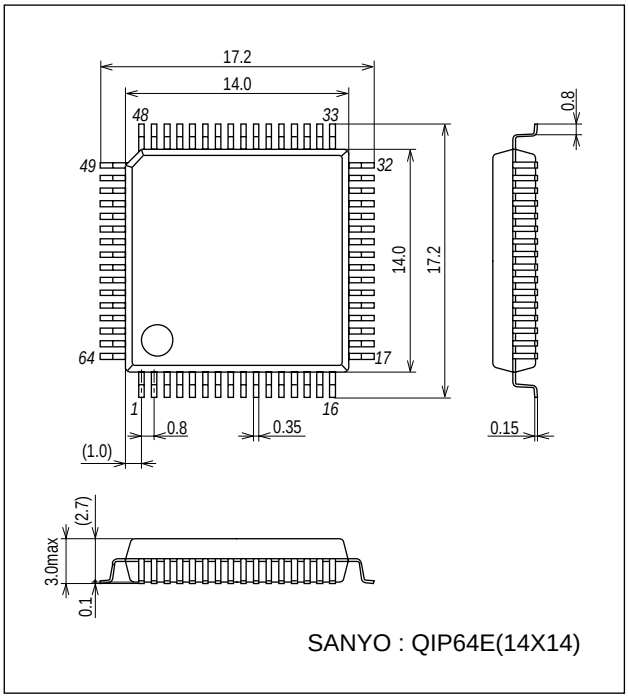
Maker		Model	Supported version	Device
Flash Support Group, Inc. (FSG)	Single Programmer	AF9708 AF9709/AF9709B/AF9709C (Including Ando Electric Co., Ltd. models)	Rev 03.04 or later	LC87F2932A
Flash Support Group, Inc. (FSG) + SANYO (Note 1)	In-circuit Programmer	AF9101/AF9103(Main body) (FSG models)	(Note 2)	LC87F2932A
		SIB87(Inter Face Driver) (SANYO model)		
SANYO	Single/Gang Programmer	SKK/SKK Type B (SANYO FWS)	Application Version 1.04 or later Chip Data Version 2.15 or later	LC87F2924
	In-circuit/Gang Programmer	SKK-DBG Type B (SANYO FWS)		

Note1: On-board-programmer from FSG (AF9101/AF9103) and serial interface driver from SANYO (SIB87) together can give a PC-less, standalone on-board-programming capabilities.

Note2: It needs a special programming devices and applications depending on the use of programming environment. Please ask FSG or SANYO for the information.

Package Dimensions

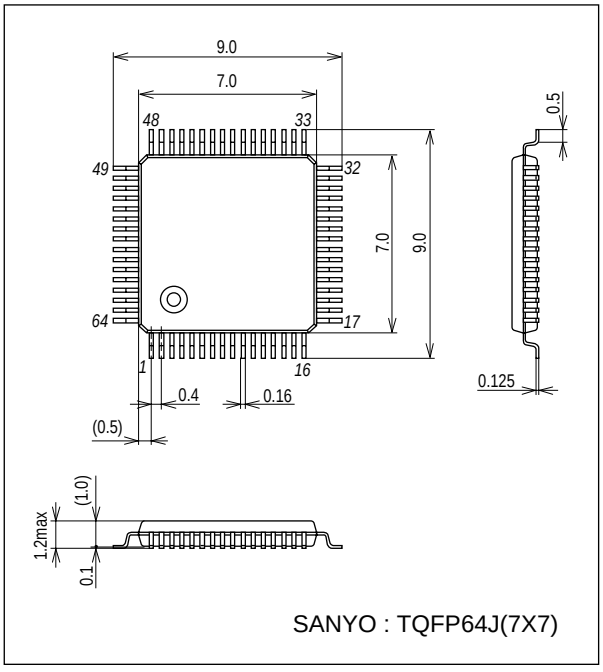
unit : mm (typ)
3159A



SANYO : QIP64E(14X14)

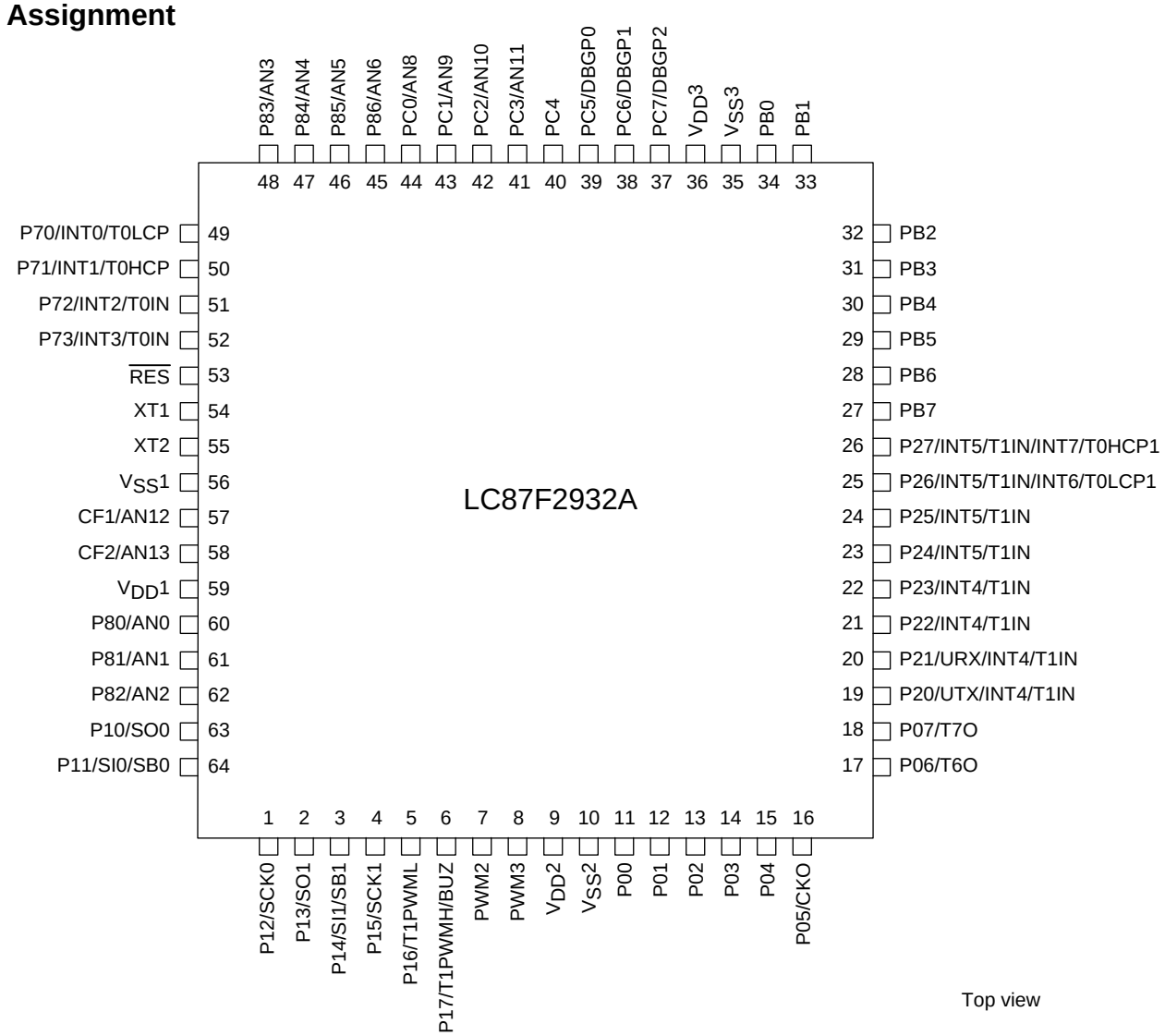
Package Dimensions

unit : mm (typ)
3289



SANYO : TQFP64J(7X7)

Pin Assignment



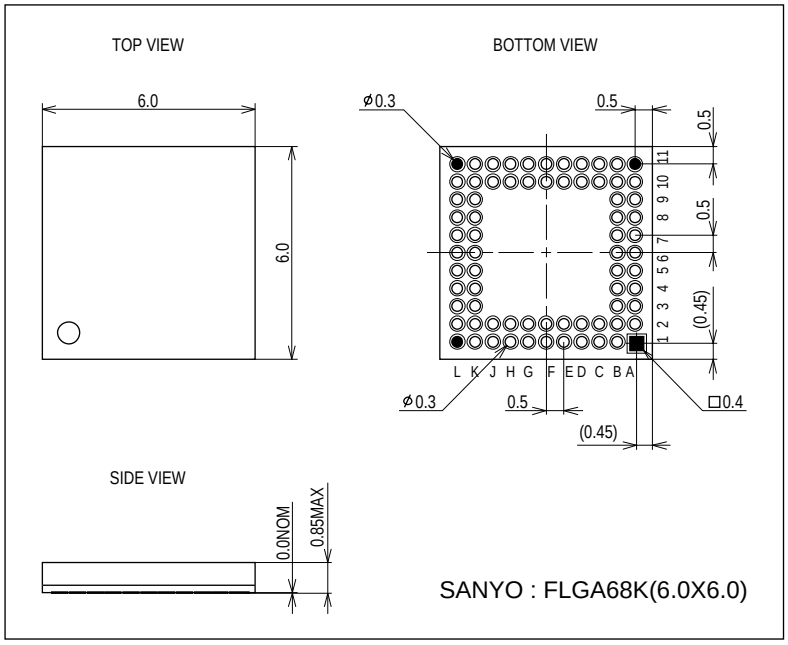
Top view

Note: Port P30, p31, p32, p33 are not available in the above package.

SANYO: QIP64E(14 × 14) "Lead-free Type"
SANYO: TQFP64J(7 × 7) "Lead-free Type"

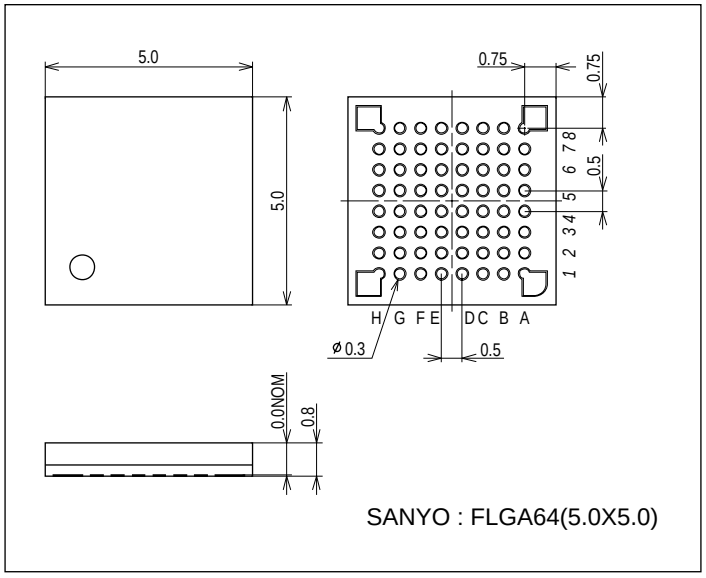
Package Dimensions

unit : mm (typ)
3326

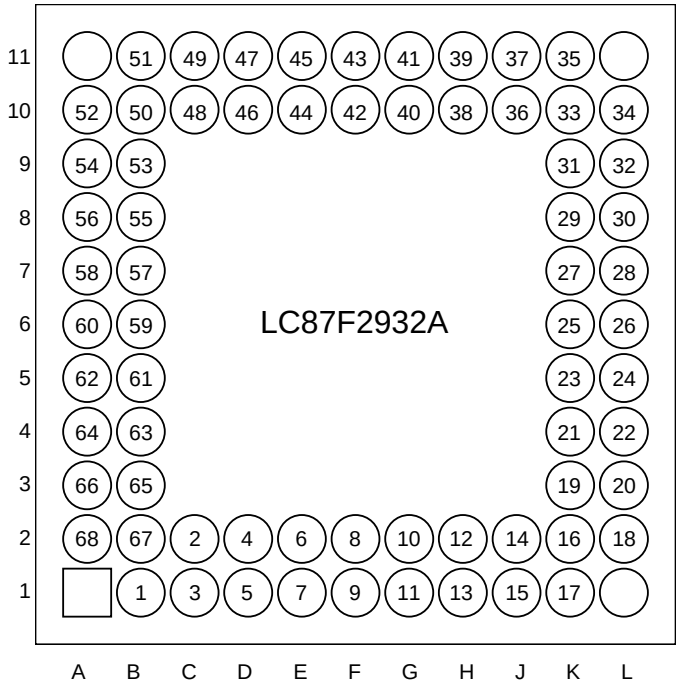


Package Dimensions

unit : mm (typ)
3328



Pin Assignments



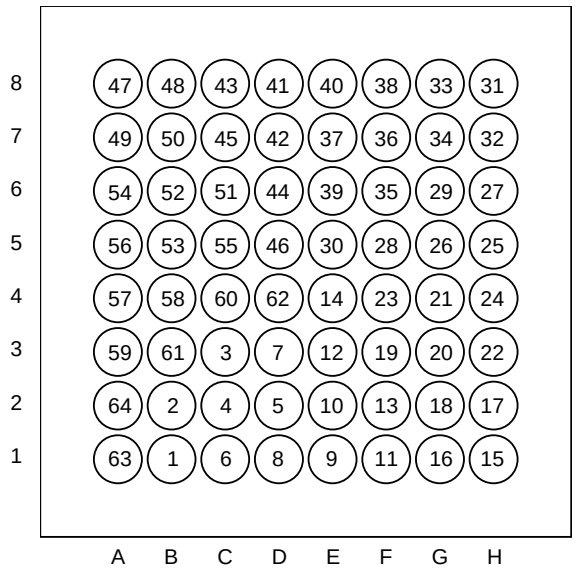
Top view

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	P12/SCK0	18	P06/T6O	35	PB1	52	P70/INT0/T0LCP
2	P13/SO1	19	P07/T7O	36	PB0	53	P71/INT1/T0HCP
3	P14/SI1/SB1	20	P20/UTX/INT4/T1IN	37	$V_{SS}3$	54	P72/INT2/T0IN
4	P15/SCK1	21	P21/URX/INT4/T1IN	38	$V_{DD}3$	55	P73/INT3/T0IN
5	P16/T1PWML	22	P22/INT4/T1IN	39	PC7/DBGP2	56	$\overline{RES}$
6	P17/T1PWMH/BUZ	23	P23/INT4/T1IN	40	PC6/DBGP1	57	XT1
7	PWM2	24	P24/INT5/T1IN	41	PC5/DBGP0	58	XT2
8	PWM3	25	P25/INT5/T1IN	42	PC4	59	$V_{SS}1$
9	$V_{DD}2$	26	P26/INT5/T1IN/INT6/TOLCP1	43	PC3/AN11	60	CF1/AN12
10	$V_{SS}2$	27	P27/INT5/T1IN/INT7/T0HCP1	44	PC2/AN10	61	CF2/AN13
11	P00	28	PB7	45	PC1/AN9	62	$V_{DD}1$
12	P01	29	PB6	46	PC0/AN8	63	P80/AN0
13	P02	30	PB5	47	P86/AN6	64	P81/AN1
14	P03	31	PB4	48	P85/AN5	65	P82/AN2
15	P04	32	PB3	49	P84/AN4	66	P10/SO0
16	P05/CKO	33	PB2	50	P83/AN3	67	P11/SI0/SB0
17	P30	34	P31	51	P32	68	P33

Note: A1, A11, L1, L11 are dummy terminals for the package.
These terminals need to be bonded with foot pattern for the secure bonding of the package.

SANYO: FLGA68K(6.0 × 6.0) "Lead-free Type"

LC87F2932A



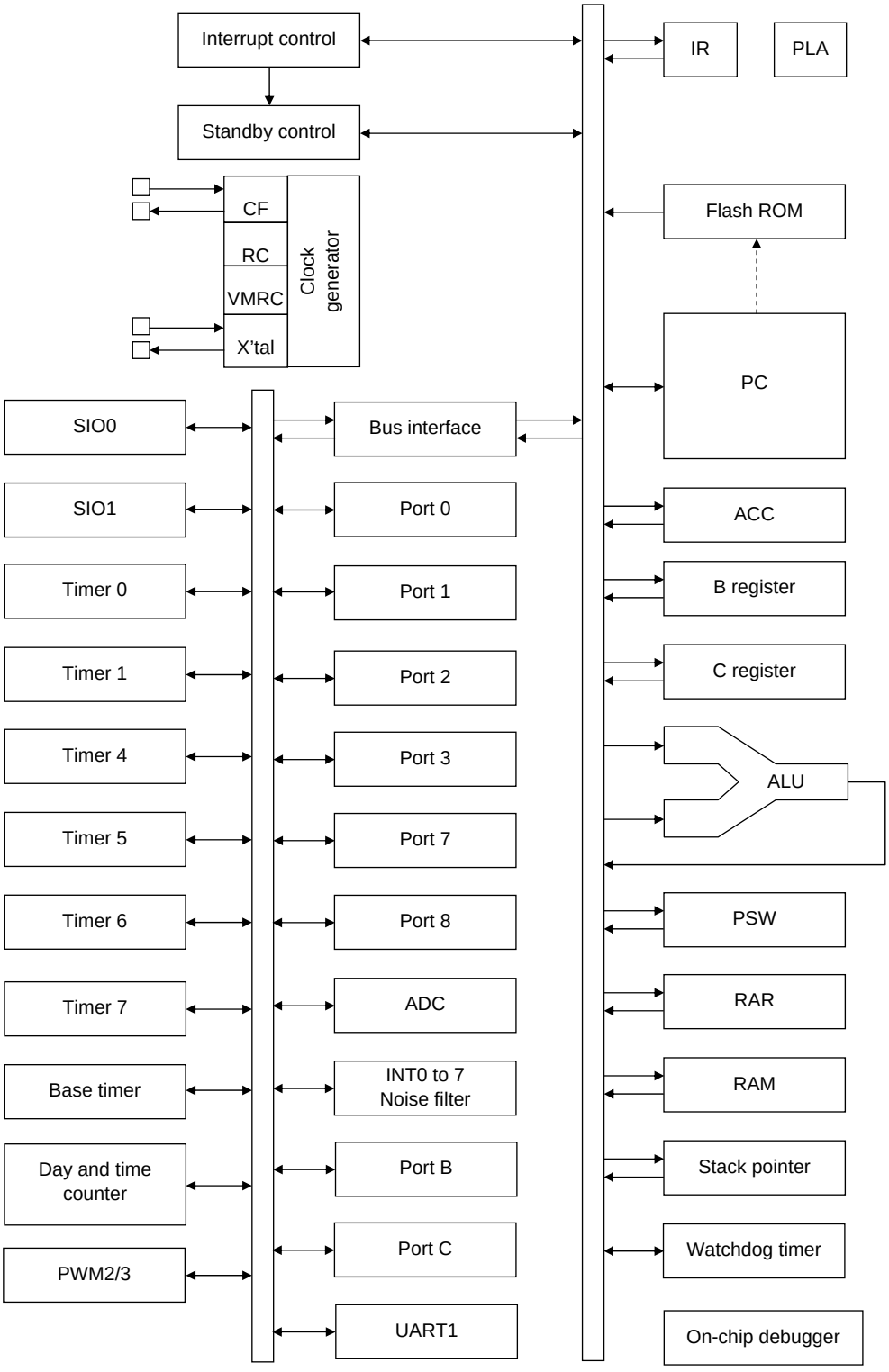
Top view

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	P12/SCK0	17	P06/T6O	33	PB1	49	P70/INT0/T0LCP
2	P13/SO1	18	P07/T7O	34	PB0	50	P71/INT1/T0HCP
3	P14/SI1/SB1	19	P20/UTX/INT4/T1IN	35	$V_{SS}3$	51	P72/INT2/T0IN
4	P15/SCK1	20	P21/URX/INT4/T1IN	36	$V_{DD}3$	52	P73/INT3/T0IN
5	P16/T1PWML	21	P22/INT4/T1IN	37	PC7/DBGP2	53	$\overline{RES}$
6	P17/T1PWMH/BUZ	22	P23/INT4/T1IN	38	PC6/DBGP1	54	XT1
7	PWM2	23	P24/INT5/T1IN	39	PC5/DBGP0	55	XT2
8	PWM3	24	P25/INT5/T1IN	40	PC4	56	$V_{SS}1$
9	$V_{DD}2$	25	P26/INT5/T1IN/INT6/T0LCP1	41	PC3/AN11	57	CF1/AN12
10	$V_{SS}2$	26	P27/INT5/T1IN/INT7/T0HCP1	42	PC2/AN10	58	CF2/AN13
11	P00	27	PB7	43	PC1/AN9	59	$V_{DD}1$
12	P01	28	PB6	44	PC0/AN8	60	P80/AN0
13	P02	29	PB5	45	P86/AN6	61	P81/AN1
14	P03	30	PB4	46	P85/AN5	62	P82/AN2
15	P04	31	PB3	47	P84/AN4	63	P10/SO0
16	P05/CKO	32	PB2	48	P83/AN3	64	P11/SI0/SB0

Note: Port P30, p31, p32, p33 are not available in the above package.

SANYO: FLGA64(5.0 × 5.0) “Lead-free Type”

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$
$V_{SS}2$
$V_{SS}3$</td><td>-</td><td>-power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}1$
$V_{DD}2$
$V_{DD}3$</td><td>-</td><td>+power supply pin</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• HOLD reset input
• Port 0 interrupt input
• Shared pins
P05: Clock output (system clock/can selected from sub clock)
P06: Timer 6 toggle output
P07: Timer 7 toggle output</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Shared pins
P10: SIO0 data output
P11: SIO0 data input/bus I/O
P12: SIO0 clock I/O
P13: SIO1 data output
P14: SIO1 data input/bus I/O
P15: SIO1 clock I/O
P16: Timer 1PWML output
P17: Timer 1PWMH output/beeper output</td><td>Yes</td></tr>
<tr><td>Port 2
P20 to P27</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Shared pins
P20: UART transmit
P21: UART receive
P26: INT6 input/HOLD reset input/timer 0L capture 1 input
P27: INT7 input/ HOLD reset input/timer 0H capture 1 input
P20 to P23: INT4 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input
P24 to P27: INT5 input/HOLD reset input/timer 1 event input/timer 0L capture input/ timer 0H capture input
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT5</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT6</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT7</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>Yes</td></tr>
<tr><td>Port 3
P30 to P33</td><td>I/O</td><td>• 4-bit I/O port
(These ports are available in FLGA68K(6.0×6.0) package only.)
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.</td><td>Yes</td></tr>
</table>

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<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7
P70 to P73</td><td>I/O</td><td>• 4-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Shared pins
P70: INT0 input/HOLD reset input/timer 0L capture input/watchdog timer output
P71: INT1 input/HOLD reset input/timer 0H capture input
P72: INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input/
High speed clock counter input
P73: INT3 input (with noise filter)/timer 0 event input/timer 0H capture input
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>No</td></tr>
<tr><td>Port 8
P80 to P86</td><td>I/O</td><td>• 7-bit I/O port
• I/O specifiable in 1-bit units
• Shared pins
AD converter input port: AN0 (P80) to AN6 (P86)</td><td>No</td></tr>
<tr><td>PWM2
PWM3</td><td>I/O</td><td>• PWM2 and PWM3 output ports
• General-purpose I/O available</td><td>No</td></tr>
<tr><td>Port B
PB0 to PB7</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1 bit units.</td><td>Yes</td></tr>
<tr><td>Port C
PC0 to PC7</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units
• Pull-up resistors can be turned on and off in 1-bit units.
• Shared pins
AD converter input port: AN8 (PC0) to AN11 (PC3)
On-chip debugger pins: DBGP0 to DBGP2 (PC5 to PC7)</td><td>Yes</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>Input</td><td>Reset pin</td><td>No</td></tr>
<tr><td>XT1</td><td>Input</td><td>• 32.768kHz crystal oscillator input pin
• Shared pins
General-purpose input port</td><td>No</td></tr>
<tr><td>XT2</td><td>I/O</td><td>• 32.768kHz crystal oscillator output pin
• Shared pins
General-purpose I/O port</td><td>No</td></tr>
<tr><td>CF1</td><td>Input</td><td>• Ceramic resonator input pin
• Shared pins
General-purpose input port
AD converter input port: AN12</td><td>No</td></tr>
<tr><td>CF2</td><td>I/O</td><td>• Ceramic resonator output pin
• Shared pins
General-purpose I/O port
AD converter input port: AN13</td><td>No</td></tr>
</table>

On-chip Debugger Pin Connection Requirements

For the treatment of the on-chip debugger pins, refer to the separately available documents entitled “RD87 On-chip Debugger Installation Manual”

Recommended Unused Pin Connections

Port Name	Recommended Unused Pin Connections	
	Board	Software
P00 to P07	Open	Output low
P10 to P17	Open	Output low
P20 to P27	Open	Output low
P30 to P33	Open	Output low
P70 to P73	Open	Output low
P80 to P86	Open	Output low
PWM2,PWM3	Open	Output low
PB0 to PB7	Open	Output low
PC0 to PC6	Open	Output low
PC7	Pulled low with a 100kΩ resistor or less	Output disable
XT1	Pulled low with a 100kΩ resistor or less	-
XT2	Open	Output low
CF1	Pulled low with a 100kΩ resistor or less	-
CF2	Open	Output low

Port Output Types

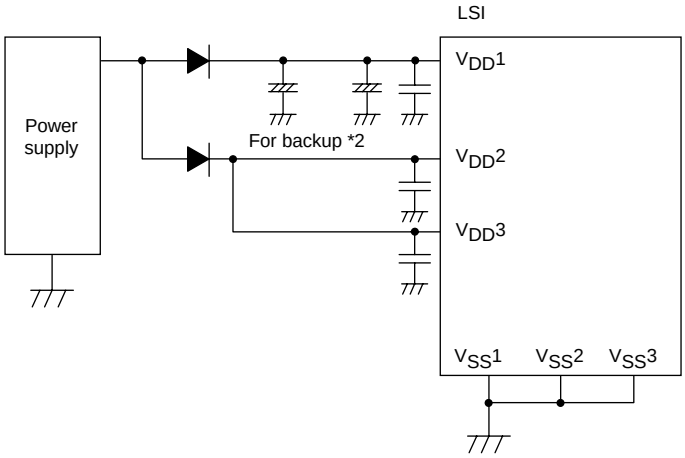
The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P10 to P17	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P27	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P33	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	-	No	CMOS	Programmable
P80 to P86	-	No	Nch-open drain	No
PWM2, PWM3	-	No	CMOS	No
PB0 to PB7	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PC0 to PC7	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
XT1	-	No	Input for 32.768kHz crystal oscillator (Input only)	No
XT2	-	No	Output for 32.768kHz crystal oscillator (Nch-open drain when in general-purpose output mode)	No
CF1	-	No	Input for ceramic oscillator (Input only)	No
CF2	-	No	Output for ceramic oscillator (Nch-open drain when in general-purpose output mode)	No

User Option Table

Option Name	Option to be Applied on	Flash-ROM Version	Option Selected in Units of	Option Selection
Port output type	P00 to P07	○	1 bit	CMOS
				Nch-open drain
	P10 to P17	○	1 bit	CMOS
				Nch-open drain
	P20 to P27	○	1 bit	CMOS
				Nch-open drain
	P30 to P33	○	1 bit	CMOS
				Nch-open drain
	PB0 to PB7	○	1 bit	CMOS
				Nch-open drain
	PC0 to PC7	○	1 bit	CMOS
				Nch-open drain
Program start address	-	○	-	00000h
				07E00h

*1: Connect the IC as shown below to minimize the noise input to the $V_{DD}1$ pin.
Be sure to electrically short the $V_{SS}1$, $V_{SS}2$, and $V_{SS}3$ pins.



*2: The internal memory is sustained by $V_{DD}1$. If none of $V_{DD}2$ and $V_{DD}3$ are backed up, the high level output at the ports are unstable in the HOLD backup mode, allowing through current to flow into the input buffer and thus shortening the backup time.
Make sure that the port outputs are held at the low level in the HOLD backup mode.

Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1$, $V_{DD}2$, $V_{DD}3$	$V_{DD}1=V_{DD}2=V_{DD}3$		-0.3		+6.5	V
Input voltage		V_I(1)	XT1, CF1			-0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}(1)	Ports 0, 1, 2, 3, 7, 8 Ports B, C PWM2, PWM3, XT2, CF2			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 1, 2, 3 Ports B, C	CMOS output select Per 1 applicable pin		-10			mA
		IOPH(2)	PWM2, PWM3	Per 1 applicable pin		-20			
		IOPH(3)	P71 to P73	Per 1 applicable pin		-5			
	Mean output current (Note 1-1)	IOMH(1)	Ports 0, 1, 2, 3 Ports B, C	CMOS output select Per 1 applicable pin		-7.5			
		IOMH(2)	PWM2, PWM3	Per 1 applicable pin		-10			
		IOMH(3)	P71 to P73	Per 1 applicable pin		-3			
	Total output current	ΣIOAH(1)	P71 to P73, P32	Total of all applicable pins		-10			
		ΣIOAH(2)	Port 1, P33 PWM2, PWM3	Total of all applicable pins		-25			
		ΣIOAH(3)	Ports 0, 2, P30	Total of all applicable pins		-25			
		ΣIOAH(4)	Ports 0, 1, 2, P30, PWM2, PWM3, P33	Total of all applicable pins		-45			
		ΣIOAH(5)	Port B, P31	Total of all applicable pins		-25			
		ΣIOAH(6)	Port C	Total of all applicable pins		-25			
		ΣIOAH(7)	Ports B, C, P31	Total of all applicable pins		-45			
Low level output current	Peak output current	IOPL(1)	P02 to P07 Ports 1, 2, 3, B, C PWM2, PWM3	Per 1 applicable pin				20	
		IOPL(2)	P00, P01	Per 1 applicable pin				30	
		IOPL(3)	Ports 7, 8, XT2, CF2	Per 1 applicable pin				10	
	Mean output current (Note 1-1)	IOML(1)	P02 to P07 Ports 1, 2, 3, B, C PWM2, PWM3	Per 1 applicable pin				15	
		IOML(2)	P00, P01	Per 1 applicable pin				20	
		IOML(3)	Ports 7, 8 XT2, CF2	Per 1 applicable pin				7.5	
	Total output current	ΣIOAL(1)	Port 7, P32 P83 to P86, XT2, CF2	Total of all applicable pins				15	
		ΣIOAL(2)	P80 to P82	Total of all applicable pins				15	
		ΣIOAL(3)	Ports 7, 8, P32 XT2, CF2	Total of all applicable pins				20	
		ΣIOAL(4)	Port 1, P33 PWM2, PWM3	Total of all applicable pins				45	
		ΣIOAL(5)	Ports 0, 2, P30	Total of all applicable pins				45	
		ΣIOAL(6)	Ports 0, 1, 2 P30, P33 PWM2, PWM3	Total of all applicable pins				80	
		ΣIOAL(7)	Port B, P31	Total of all applicable pins				45	
		ΣIOAL(8)	Port C	Total of all applicable pins				45	
		ΣIOAL(9)	Ports B, C, P31	Total of all applicable pins				80	

Note 1-1: The mean output current is a mean value measured over 100ms.

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Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Power dissipation	Pd max	QIP64E(14×14)	Ta=-40 to +85°C				292	mW
		TQFP64J(7×7)					133	
		FLGA68K(6.0×6.0)					96	
		FLGA64(5.0×5.0)					91	
Operating ambient temperature	Topr				-40		+85	°C
Storage ambient temperature	Tstg				-55		+125	

Allowable Operating Range at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	$V_{DD}(1)$	$V_{DD}1=V_{DD}2=V_{DD}3$	0.245µs ≤ tCYC ≤ 200µs		3.0		5.5	V
			0.367µs ≤ tCYC ≤ 200µs		2.5		5.5	
			0.681µs ≤ tCYC ≤ 200µs		2.2		5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1=V_{DD}2=V_{DD}3$	RAM and register contents sustained in HOLD mode.		2.0		5.5	
High level input voltage	$V_{IH}(1)$	Ports 1, 2 P71 to P73 P70 port input/ interrupt side		2.2 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(2)$	Ports 0, 3, 8, B, C PWM2, PWM3		2.2 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(3)$	Port 70 watchdog timer side		2.2 to 5.5	$0.9V_{DD}$		V_{DD}	
	$V_{IH}(4)$	$\overline{\text{XT1}}$, XT2, CF1, CF2, $\overline{\text{RES}}$		2.2 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 1, 2 P71 to P73 P70 port input/ interrupt side		4.0 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
				2.2 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(2)$	Ports 0, 3, 8, B, C PWM2, PWM3		4.0 to 5.5	V_{SS}		$0.15V_{DD}$ +0.4	
				2.2 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(3)$	Port 70 watchdog timer side		2.2 to 5.5	V_{SS}		$0.8V_{DD}$ -1.0	
	$V_{IL}(4)$	$\overline{\text{XT1}}$, XT2, CF1, CF2, $\overline{\text{RES}}$		2.2 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-2)	tCYC			3.0 to 5.5	0.245		200	µs
				2.5 to 5.5	0.367		200	
				2.2 to 5.5	0.681		200	
External system clock frequency	FEXCF(1)	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty =50±5%	3.0 to 5.5	0.1		12	MHz
				2.5 to 5.5	0.1		8	
				2.2 to 5.5	0.1		4	
			• CF2 pin open • System clock frequency division ratio=1/2	3.0 to 5.5	0.2		24.4	
				2.5 to 5.5	0.2		16	
				2.2 to 5.5	0.2		8	

Note 2-1: V_{DD} must be held greater than or equal to 3.0V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

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Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	• 12MHz ceramic oscillation • See Fig. 1.	3.0 to 5.5		12		MHz
	FmCF(2)	CF1, CF2	• 8MHz ceramic oscillation • See Fig. 1.	2.5 to 5.5		8		
	FmCF(3)	CF1, CF2	• 4MHz ceramic oscillation • See Fig. 1.	2.2 to 5.5		4		
	FmRC		Internal RC oscillation	2.2 to 5.5	0.3	1.0	2.0	
	FmVMRC(1)		• Frequency variable RC source oscillation • When VMRAJ2 to 0=4, VMFAJ2 to 0=0, VMSL4M=0	2.2 to 5.5		10		
	FmVMRC(2)		• Frequency variable RC source oscillation • When VMRAJ2 to 0=4, VMFAJ2 to 0=0, VMSL4M=1	2.2 to 5.5		4		
	FsX'tal	XT1, XT2	• 32.768kHz crystal oscillation • See Fig. 2.	2.2 to 5.5		32.768		kHz
Frequency variable RC oscillation usable range	OpVMRC(1)		When VMSL4M=0	2.2 to 5.5	8	10	12	MHz
	OpVMRC(2)		When VMSL4M=1	2.2 to 5.5	3.5	4	4.5	
Frequency variable RC oscillation adjustment range	VmADJ(1)		Each step of VMRAJn (Wide range)	2.2 to 5.5	8	24	64	%
	VmADJ(2)		Each step of VMFAJn (Small range)	2.2 to 5.5	1	4	8	

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Electrical Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 2, 3 Ports 7, 8 Ports B, C $\overline{RES}$ PWM2, PWM3	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (Including output Tr's off leakage current)	2.2 to 5.5			1	µA
	$I_{IH}(2)$	XT1, XT2, CF1, CF2	For input port specification $V_{IN}=V_{DD}$	2.2 to 5.5			1	
	$I_{IH}(3)$	CF1	$V_{IN}=V_{DD}$	2.2 to 5.5			15	
Low level input current	$I_{IL}(1)$	Ports 0, 1, 2, 3 Ports 7, 8 Ports B, C $\overline{RES}$ PWM2, PWM3	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (Including output Tr's off leakage current)	2.2 to 5.5	-1			
	$I_{IL}(2)$	XT1, XT2, CF1, CF2	For input port specification $V_{IN}=V_{SS}$	2.2 to 5.5	-1			
	$I_{IL}(3)$	CF1	$V_{IN}=V_{SS}$	2.2 to 5.5	-15			
High level output voltage	$V_{OH}(1)$	Ports 0, 1, 2, 3 Ports B, C	I_{OH}=-1mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(3)$		I_{OH}=-0.2mA	2.2 to 5.5	V_{DD}-0.4			
	$V_{OH}(4)$	P71 to P73	I_{OH}=-0.4mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(5)$		I_{OH}=-0.2mA	2.2 to 5.5	V_{DD}-0.4			
	$V_{OH}(6)$	PWM2, PWM3	I_{OH}=-10mA	4.5 to 5.5	V_{DD}-1.5			
	$V_{OH}(7)$		I_{OH}=-1.6mA	3.0 to 5.5	V_{DD}-0.4			
	$V_{OH}(8)$		I_{OH}=-1mA	2.2 to 5.5	V_{DD}-0.4			
Low level output voltage	$V_{OL}(1)$	Ports 0, 1, 2, 3 Ports B, C PWM2, PWM3	I_{OL}=10mA	4.5 to 5.5			1.5	
	$V_{OL}(2)$		I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(3)$		I_{OL}=1mA	2.2 to 5.5			0.4	
	$V_{OL}(4)$	Ports 7, 8 XT2, CF2	I_{OL}=1.6mA	3.0 to 5.5			0.4	
	$V_{OL}(5)$		I_{OL}=1mA	2.2 to 5.5			0.4	
	$V_{OL}(6)$	P00, P01	I_{OL}=30mA	4.5 to 5.5			1.5	
	$V_{OL}(7)$		I_{OL}=5mA	3.0 to 5.5			0.4	
	$V_{OL}(8)$		I_{OL}=2.5mA	2.2 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 3 Ports 7, B, C	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			2.2 to 5.5	18	50	150	
Hysteresis voltage	VHYS	$\overline{RES}$ Ports 1, 2, 7		2.2 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	For pins other than that under test: $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	2.2 to 5.5		10		pF

Serial Input/Output Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

1. SIO0 Serial I/O Characteristics (Note 4-1-1)

Parameter			Symbol	Pin/Remarks	Conditions	Specification				
						V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.	2.2 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
			tSCKHA(1)		• Continuous data transmission/reception mode • See Fig. 6. • (Note 4-1-2)		4			
	Output clock	Frequency	tSCK(2)	SCK0(P12)	• CMOS output selected • See Fig. 6.	2.2 to 5.5	4/3			
		Low level pulse width	tSCKL(2)				1/2			tSCK
		High level pulse width	tSCKH(2)				1/2			
			tSCKHA(2)		• Continuous data transmission/reception mode • CMOS output selected • See Fig. 6.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
Serial input	Data setup time		tsDI(1)	SB0(P11), SI0(P11)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.2 to 5.5	0.03			µs
	Data hold time		thDI(1)			2.2 to 5.5	0.03			
Serial output	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	• Continuous data transmission/reception mode • (Note 4-1-3)	2.2 to 5.5			(1/3)tCYC +0.05	
			tdD0(2)		• Synchronous 8-bit mode • (Note 4-1-3)	2.2 to 5.5			1tCYC +0.05	
	Output clock		tdD0(3)		(Note 4-1-3)	2.2 to 5.5			(1/3)tCYC +0.15	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SI0RUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

2. SIO1 Serial I/O Characteristics (Note 4-2-1)

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(3)	SCK1(P15)	See Fig. 6.	2.2 to 5.5	2			tCYC
		Low level pulse width	tSCKL(3)				1			
		High level pulse width	tSCKH(3)				1			
	Output clock	Frequency	tSCK(4)	SCK1(P15)	• CMOS output selected • See Fig. 6.	2.2 to 5.5	2			tSCK
		Low level pulse width	tSCKL(4)				1/2			
		High level pulse width	tSCKH(4)				1/2			
Serial input	Data setup time		tsDI(2)	SB1(P14), SI1(P14)	• Must be specified with respect to rising edge of SIOCLK. • See Fig. 6.	2.2 to 5.5	0.03			µs
	Data hold time		thDI(2)			2.2 to 5.5	0.03			
Serial output	Output delay time		tdD0(4)	SO1(P13), SB1(P14)	• Must be specified with respect to falling edge of SIOCLK. • Must be specified as the time to the beginning of output state change in open drain output mode. • See Fig. 6.	2.2 to 5.5			(1/3)tCYC +0.05	

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P72), INT3(P73) when noise filter not used, INT4(P20 to P23), INT5(P24 to P27), INT6(P26), INT7(P27)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.2 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P73) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.2 to 5.5	2			
	tPIH(3) tPIL(3)	INT3(P73) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.2 to 5.5	64			
	tPIH(4) tPIL(4)	INT3(P73) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.2 to 5.5	256			
	tPIL(5)	$\overline{RES}$	Resetting is enabled.	2.2 to 5.5	200			µs

AD Converter Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN0(P80) to AN6(P86), AN8(PC0), AN9(PC1), AN10(PC2), AN11(PC3), AN12(CF1), AN13(CF2)		3.0 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	tCAD		AD conversion time=32×tCYC (when ADCR2=0) (Note 6-2)	4.5 to 5.5	15.68 (tCYC= 0.49µs)		97.92 (tCYC= 3.06µs)	µs
				3.0 to 5.5	21.8 (tCYC= 0.681µs)		97.92 (tCYC= 3.06µs)	
			AD conversion time=64×tCYC (when ADCR2=1) (Note 6-2)	4.5 to 5.5	18.82 (tCYC= 0.294µs)		97.92 (tCYC= 1.53µs)	
				3.0 to 5.5	43.6 (tCYC= 0.681µs)		97.92 (tCYC= 1.53µs)	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		V_{DD}	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	µA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

Note 6-1: The quantization error (±1/2LSB) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued to the time the complete digital value corresponding to the analog input value is loaded in the required register.

Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Normal mode consumption current (Note 7-1)	IDDOP(1)	$V_{DD}1$ $=V_{DD}2$ $=V_{DD}3$	• FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		8.38	20.9	mA
	IDDOP(2)			3.0 to 3.6		4.85	11.9	
	IDDOP(3)		• FmCF=8MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 8MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		6.36	15.7	
	IDDOP(4)			3.0 to 3.6		3.64	9.1	
	IDDOP(5)			2.5 to 3.0		2.42	7.1	
	IDDOP(6)		• FmCF=4MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 4MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		2.42	6	
	IDDOP(7)			3.0 to 3.6		1.31	3.3	
	IDDOP(8)			2.2 to 3.0		0.87	2.5	
	IDDOP(9)		• FmCF=0Hz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		0.76	3.1	
	IDDOP(10)			3.0 to 3.6		0.4	1.7	
	IDDOP(11)			2.2 to 3.0		0.28	1.35	
	IDDOP(12)		• FmCF=0Hz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 10MHz with frequency variable RC oscillation • 1/1 frequency division ratio	4.5 to 5.5		8.08	20	
	IDDOP(13)			3.0 to 3.6		4.75	12	
	IDDOP(14)		• FmCF=0Hz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 4MHz with frequency variable RC oscillation • 1/1 frequency division ratio	4.5 to 5.5		4.55	11.5	
	IDDOP(15)			3.0 to 3.6		2.63	6.6	
	IDDOP(16)			2.2 to 3.0		1.72	5	
	IDDOP(17)		• FmCF=0Hz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		35.4	115	µA
	IDDOP(18)			3.0 to 3.6		18.2	65	
	IDDOP(19)			2.2 to 3.0		12.1	46	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

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Parameter	Symbol	Pin/ Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
HALT mode consumption current (Note 7-1)	IDDHALT(1)	$V_{DD}1$ =$V_{DD}2$ =$V_{DD}3$	• HALT mode • FmCF=12MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 12MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		3.71	8.2	mA
	IDDHALT(2)			3.0 to 3.6		2.06	4.6	
	IDDHALT(3)		• HALT mode • FmCF=8MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 8MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/1 frequency division ratio	4.5 to 5.5		2.68	5.9	
	IDDHALT(4)			3.0 to 3.6		1.44	3.3	
	IDDHALT(5)			2.5 to 3.0		1.03	2.5	
	IDDHALT(6)		• HALT mode • FmCF=4MHz ceramic oscillation mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 4MHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		1.18	2.65	
	IDDHALT(7)			3.0 to 3.6		0.62	1.5	
	IDDHALT(8)			2.2 to 3.0		0.41	1.1	
	IDDHALT(9)		• HALT mode • FmCF=0Hz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to internal RC oscillation • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		0.38	1.3	
	IDDHALT(10)			3.0 to 3.6		0.21	0.75	
	IDDHALT(11)			2.2 to 3.0		0.13	0.54	
	IDDHALT(12)		• HALT mode • FmCF=0Hz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 10MHz with frequency variable RC oscillation • 1/1 frequency division ratio	4.5 to 5.5		3.71	8.2	
	IDDHALT(13)			3.0 to 3.6		2.06	4.6	
	IDDHALT(14)		• HALT mode • FmCF=0Hz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • Internal RC oscillation stopped. • System clock set to 4MHz with frequency variable RC oscillation • 1/1 frequency division ratio	4.5 to 5.5		1.75	4	
	IDDHALT(15)			3.0 to 3.6		1.03	2.5	
	IDDHALT(16)			2.2 to 3.0		0.72	1.8	
	IDDHALT(17)		• HALT mode • FmCF=0Hz (oscillation stopped) • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz side • Internal RC oscillation stopped. • Frequency variable RC oscillation stopped. • 1/2 frequency division ratio	4.5 to 5.5		19.1	68	µA
	IDDHALT(18)			3.0 to 3.6		10.3	38	
	IDDHALT(19)			2.2 to 3.0		6.7	26	
HOLD mode consumption current	IDDHOLD(1)	$V_{DD}1$	• HOLD mode • CF1=V_{DD} or open (External clock mode)	4.5 to 5.5		0.1	20	
	IDDHOLD(2)			3.0 to 3.6		0.06	12	
	IDDHOLD(3)			2.2 to 3.0		0.04	8	
Timer HOLD mode consumption current	IDDHOLD(4)		• Timer HOLD mode • CF1=V_{DD} or open (External clock mode) • FsX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		16.5	58	
	IDDHOLD(5)			3.0 to 3.6		8.8	32	
	IDDHOLD(6)			2.2 to 3.0		5.2	20	

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

F-ROM Programming Characteristics at Ta = -10°C to +55°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

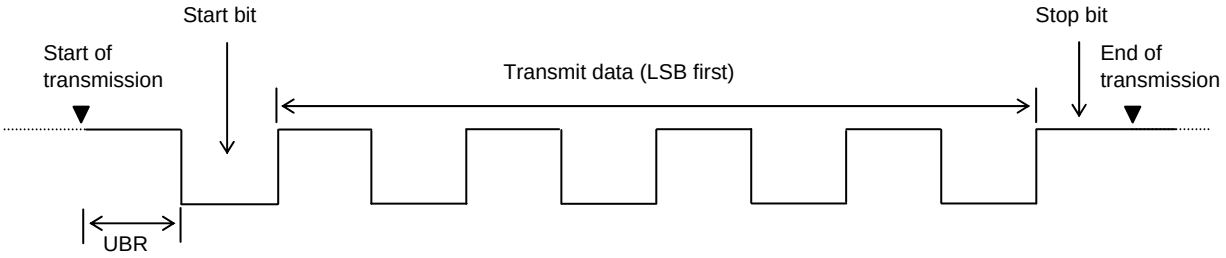
Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Without CPU current	3.0 to 5.5		5	10	mA
Programming time	tFW(1)		• Erasing	3.0 to 5.5		20	30	ms
	tFW(2)		• Programming			40	60	µs

UART (Full Duplex) Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$

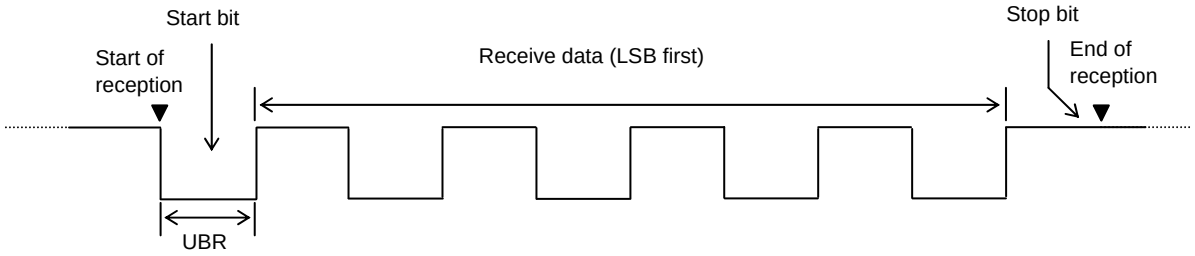
Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Transfer rate	UBR	UTX(P20), URX(P21)		2.2 to 5.5	16/3		8192/3	tCYC

Data length: 7, 8, and 9 bits (LSB first)
Stop bits: 1 bit (2-bit in continuous data transmission)
Parity bits: None

Example of Continuous 8-bit Data Transmission Mode Processing (first transmit data=55H)



Example of Continuous 8-bit Data Reception Mode Processing (first receive data=55H)



Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf1 [Ω]	Rd1 [Ω]		typ [ms]	max [ms]	
12MHz	MURATA	CSTCE12M0G52-R0	(10)	(10)	Open	680	3.0 to 5.5	0.05	0.15	Internal C1, C2
8MHz	MURATA	CSTCE8M00G52-R0	(10)	(10)	Open	1k	2.5 to 5.5	0.13	0.4	Internal C1, C2
		CSTLS8M00G53-B0	(15)	(15)	Open	1k	2.5 to 5.5	0.12	0.4	
4MHz	MURATA	CSTCR4M00G53-R0	(15)	(15)	Open	2.2k	2.2 to 5.5	0.07	0.2	Internal C1, C2
		CSTLS4M00G53-B0	(15)	(15)	Open	2.2k	2.2 to 5.5	0.05	0.15	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after V_{DD} goes above the operating voltage lower limit (see Figure 4).

Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C3 [pF]	C4 [pF]	Rf2 [Ω]	Rd2 [Ω]		typ [s]	max [s]	
32.768kHz	EPSON TOYOCOM	MC-306	18	18	Open	560k	2.2 to.5.5	1.3	3.0	Applicable CL value= 12.5pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

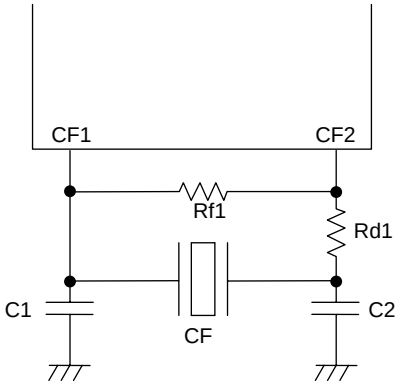


Figure 1 CF Oscillator Circuit

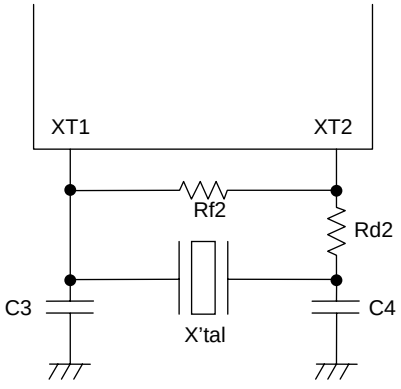


Figure 2 XT Oscillator Circuit

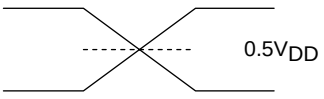
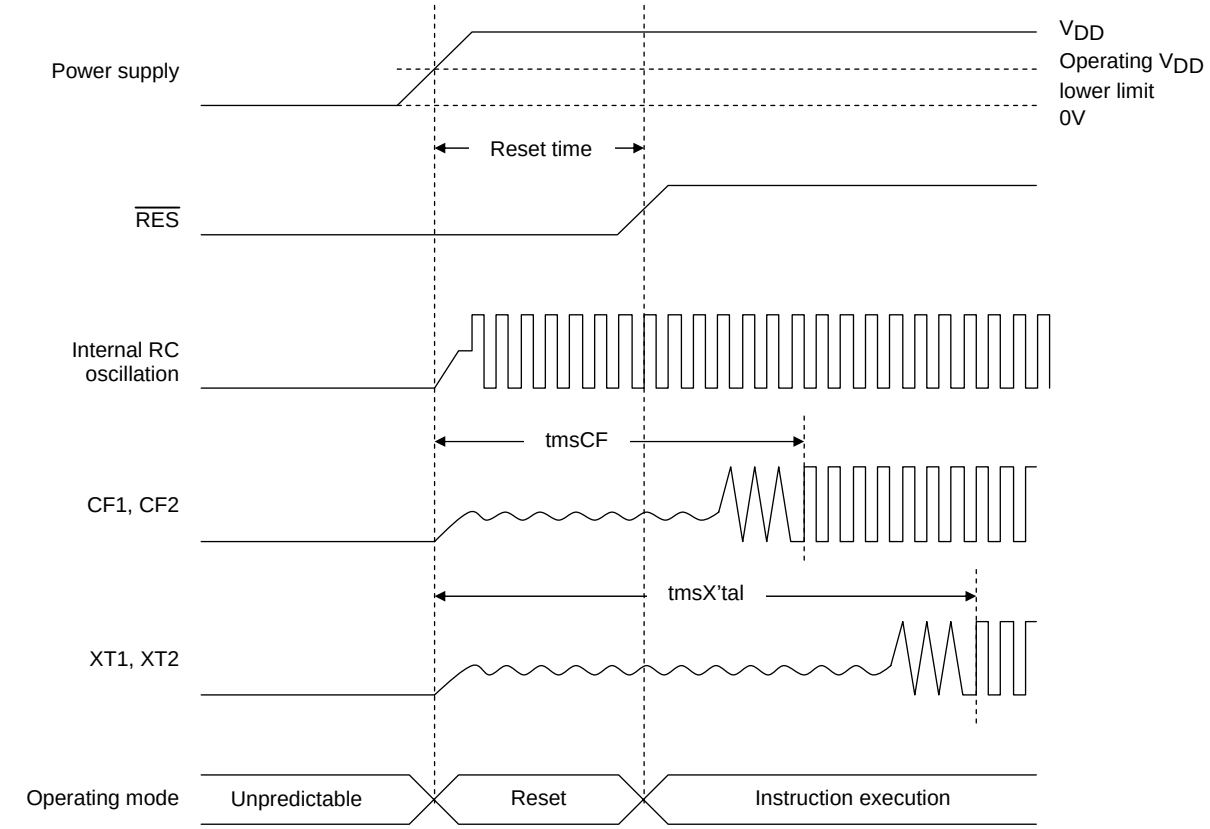
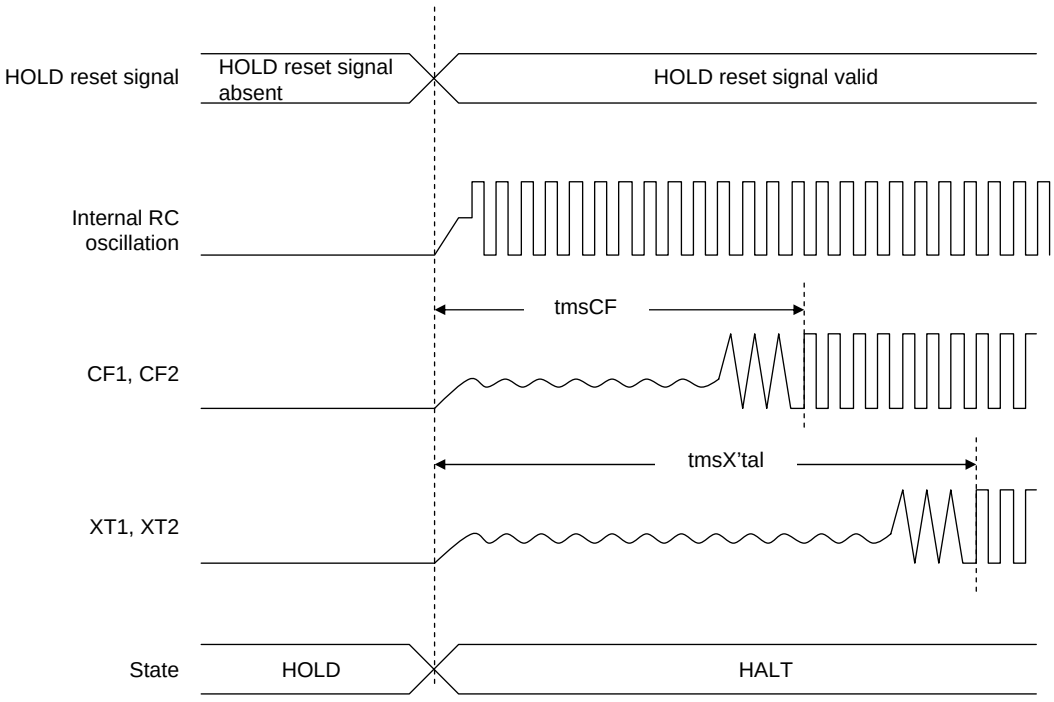


Figure 3 AC Timing Measurement Point

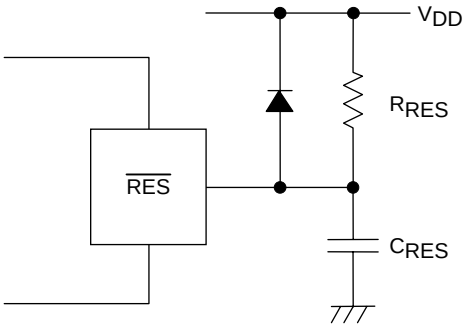


Reset Time and Oscillation Stabilization Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



Note:
Determine the value of C_{RES} and R_{RES} so that the reset signal is present for a period of 200µs after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 5 Reset Circuit

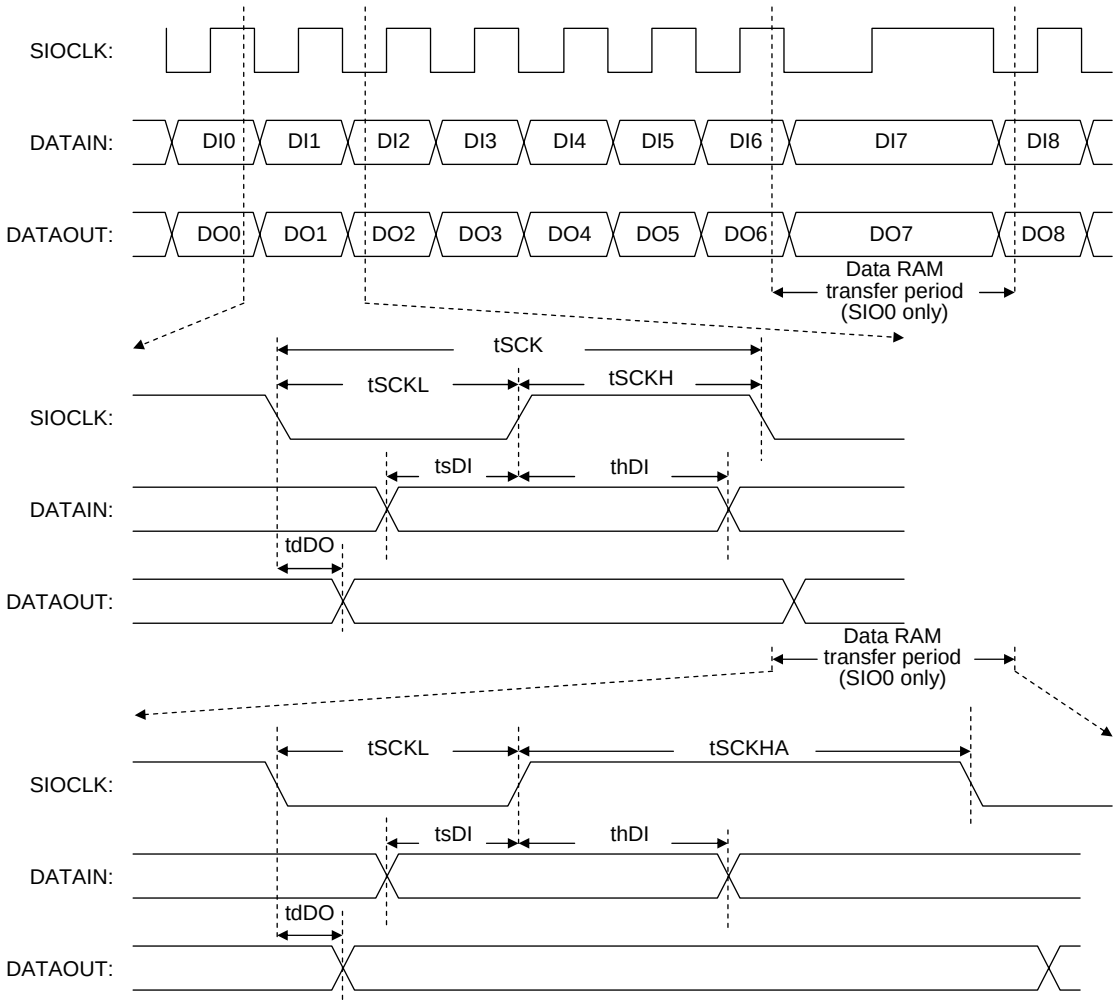


Figure 6 Serial I/O Waveforms

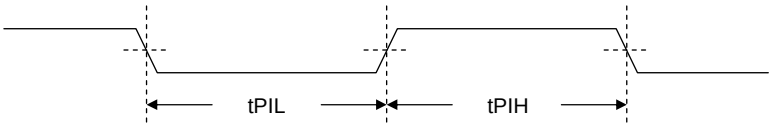


Figure 7 Pulse Input Timing Signal Waveform